

JMM4808N

30V 40A N-Channel MOSFET

Absolute Maximum Ratings

Parameter	Symbol	Limit	Unit
Drain-to-Source Voltage	V_{DS}	30	V
Gate-to-Source Voltage	V_{GS}	± 20	
Continuous Drain Current, Package Limited ($T_C = 25^\circ\text{C}$) ⁽¹⁾	I_D	40	A
Continuous Drain Current, Silicon Limited ($T_C = 25^\circ\text{C}$) ⁽¹⁾	I_D	110	
Continuous Drain Current, Silicon Limited ($T_C = 100^\circ\text{C}$) ⁽¹⁾	I_D	70	
Continuous Drain Current, Silicon Limited t ($T_A = 25^\circ\text{C}$) ^{(2), (5)}	I_D	22	
Continuous Drain Current, Silicon Limited ($T_A = 100^\circ\text{C}$) ^{(2), (5)}	I_D	14	
Pulsed Drain Current ⁽³⁾	I_{DM}	160	
Power Dissipation ($T_C = 25^\circ\text{C}$)	P_D	56	W
Linear Derating Factor	-	0.45	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy ⁽⁴⁾	E_{AS}	83.5	mJ
Avalanche Current ⁽⁴⁾	I_{AS}	26	A
Junction Temperature	T_J	-55 to 150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 to 150	

Thermal Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Junction-to-Ambient Thermal Resistance ⁽⁵⁾	R_{JA}	-	55	-	$^\circ\text{C}/\text{W}$
Junction-to-Case Thermal Resistance	R_{JC}	-	2.2	-	

Static Electrical Characteristics⁽⁶⁾

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-to-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	30	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1.0	-	2.0	
Drain-to-Source Leakage Current	I_{DSS}	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}$	-	-	1	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

Drain-to-Source On-Resistance $R_{DS(ON)}$ $V_{GS} = 10\text{V}, I_D = 10$

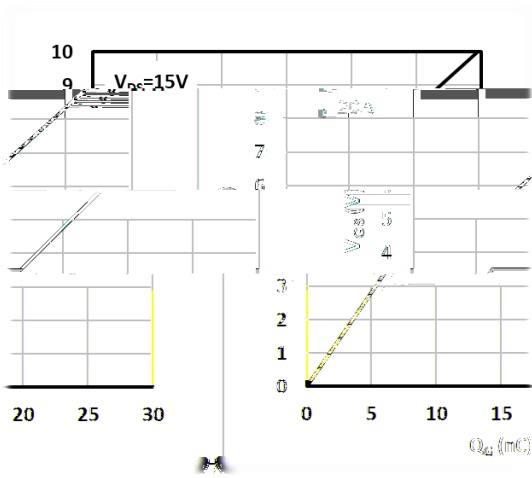


Fig.7 Gate-to-source voltage vs gate charge

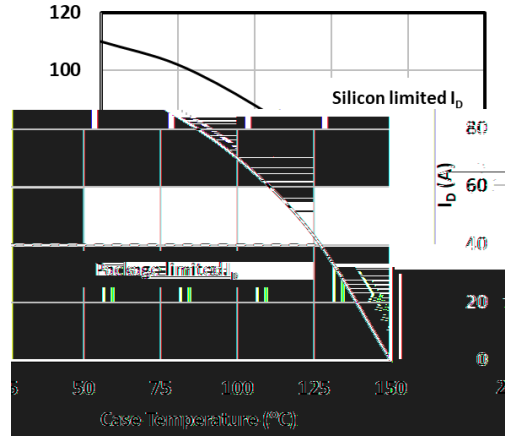


Fig.8 Maximum drain current vs. case temperature

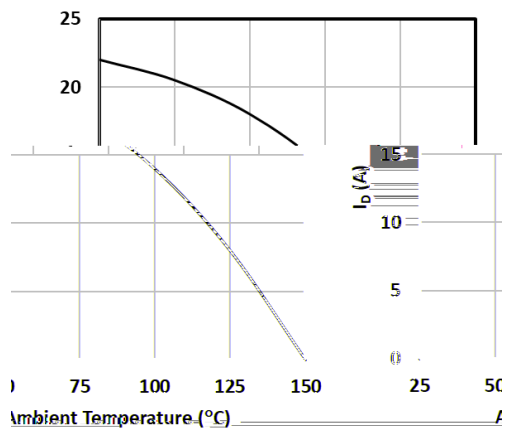
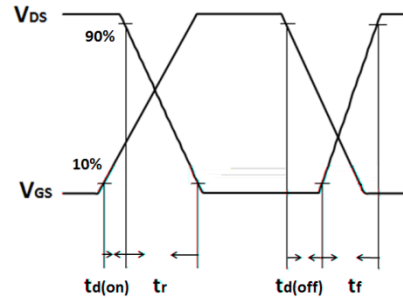
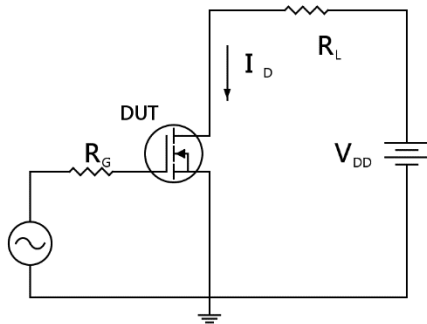
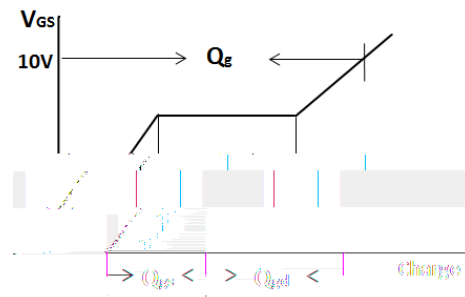
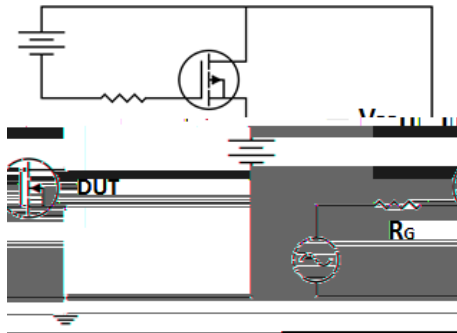


Fig. 9 Maximum drain current vs. ambient temperature

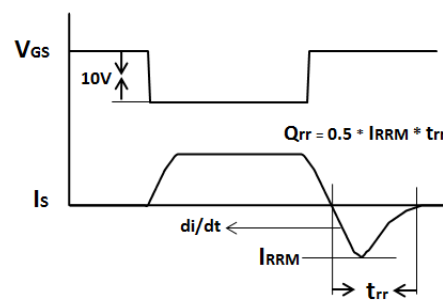
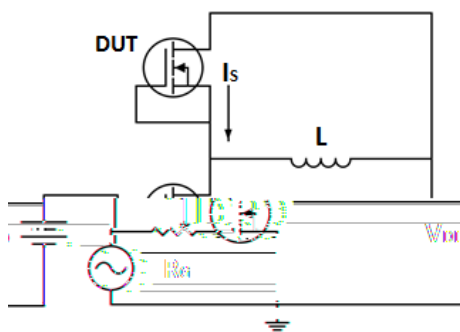
Test Circuits and Waveforms



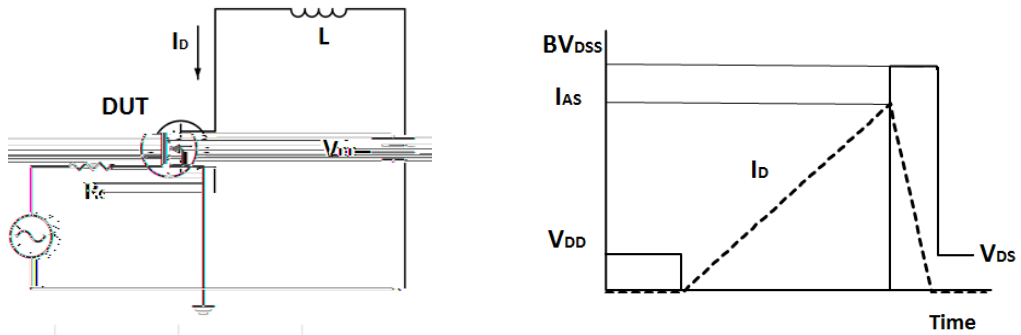
Resistive switching time test circuit & waveforms



Gate charge test circuit & waveform



Peak diode recovery dv/dt test circuit & waveforms



Unclamped inductive switching test circuit & waveforms

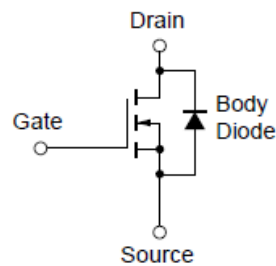
Package Drawing



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0	-	0.05
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
α	0°	-	12°

DFN5x6

Equivalent Circuit



Revision history of JMM4808N specification

Version	Change Items	Effective Date
1.00	Initial Release	09-Mar-20

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